A Novel Power Plane With Integrated Simultaneous Switching Noise Mitigation Capability Using High Impedance Surface

Telesphor Kamgaing, *Student Member, IEEE,* and Omar M. Ramahi, *Senior Member, IEEE*

***Abstract*—A novel technique for suppressing power plane resonance at microwave and radio frequencies is presented. The new concept consists of replacing one of the plates of a parallel power plane pair with a high impedance surface or electromagnetic band gap structure. The combination of this technique with a wall of RC pairs extends the lower edge of the effective bandwidth to dc, and allows resonant mode suppression up to the upper edge of the band-gap. The frequency range for noise mitigation is controlled by the geometry of the HIGP structure.**

***Index Terms*—High impedance surface (HIS), power planes, simultaneous switching noise (SSN).**

I. Introduction

TODAY'S high-speed digital systems have hundreds of gates that have to switch simultaneously. When the noise produced by the simultaneous switching of all these gates approaches the noise tolerance of static CMOS circuits, a degradation of the signal integrity can occur. In printed circuit boards (PCB), each digital gate is usually connected between two power planes representing the power supply V_{DD} and the reference plane, as shown in Fig. 1. The simultaneous switching noise (SSN) becomes acute when the noise generated by the active devices contains dominant frequency harmonics that fall within the resonant modes of the power planes. Therefore, the most effective and efficient approach to mitigating SSN is to reduce power plane resonance.

Resonance of parallel plates is traditionally mitigated by connecting decoupling capacitors (decaps) between the two plates. Previous works also showed that connecting a resistance in series with the decoupling capacitor will improve the noise mitigation [1]–[3]. These two techniques, however, have practical limitations. Although they offer excellent performance at low frequencies, they do not yield sufficient suppression beyond 500 MHz for most practical boards because the capacitors' lead inductance becomes dominant. Another technique for noise suppression consists of etching a trench around the noise source and connecting the island (isolated active device) to the rest of the board via small inductors [3]. The trench prevents the switching noise from propagating to the rest of the board. This technique, however, suffers from the limitations imposed by the dominant lead inductance of the capacitors [3].

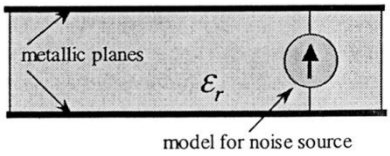

Fig. 1. Cross section view of a conventional power plane with noise source.

In a dramatic departure from previous techniques, this paper introduces a novel technique that consists of replacing one of the plates of a traditional power plane pair with a high impedance surface (HIS). The HIS structure is designed to provide a wide bandgap expanding from dc to the microwave and radio frequency ranges relevant to the PCB clock.

II. Power Plane Using High Impedance Surface

Novel HIS structures have been introduced in recent years for suppression of surface waves (see [4] and references therein). These structures support TM mode waves only at low frequencies and TE mode waves only at high frequencies. Between the two regions, there is a transition region, where the HIS behaves as a perfect magnetic conductor and supports neither TE nor TM mode waves. Applying such a structure in the parallel-plate resonant cavity for SSN suppression would require its bandgap to overlap with the high transmission band of the simple parallel-plate system. The HIS surface reported in [4] consists of hexagonal patches having a periodicity of a and center vias. Designing an HIS surface for Low frequency ($<$5 GHz) has been achieved previously by using multilayer patches to increase the fringing capacitance that together with the via inductance creates the effect of a parallel resonant circuit [4]. Despite the shifting of the center frequency into the radio frequency range, the multilayer design has a narrow bandwidth at RF frequencies, which is typically not suitable for switching noise reduction in that frequency range.

The HIS presented in this work and shown in Fig. 2 is used in place of the lower solid plane of the traditional power plane pair

Manuscript received May 27, 2002; revised July 18, 2002. This work was supported in part by Motorola, Inc. and the DoD MURI Program on Effects of Radio-Frequency Pulses on Electronic Circuits and Systems under AFOSR Grant F496200110374. The review of this letter was arranged by Assoicate Editor Dr. Ruediger Vahldieck.

T. Kamgaing is with the Motorola Semiconductor Products Sector, Inc., Digital DNA Laboratories, Tempe, AZ 85284 USA, and also with the Electrical and Computer Engineering Department, University of Maryland, College Park, MD 20742 USA (e-mail: t.kamgaing@motorola.com).

O. M. Ramahi is with the Mechanical Engineering Department, Electrical and Computer Engineering Department, and CALCE Electronic Products and Systems Center, University of Maryland, College Park, MD 20742 USA (e-mail: oramahi@calce.umd.edu; www.enme.umd.edu\∼oramahi).

Digital Object Identifier 10.1109/LMWC.2002.807713

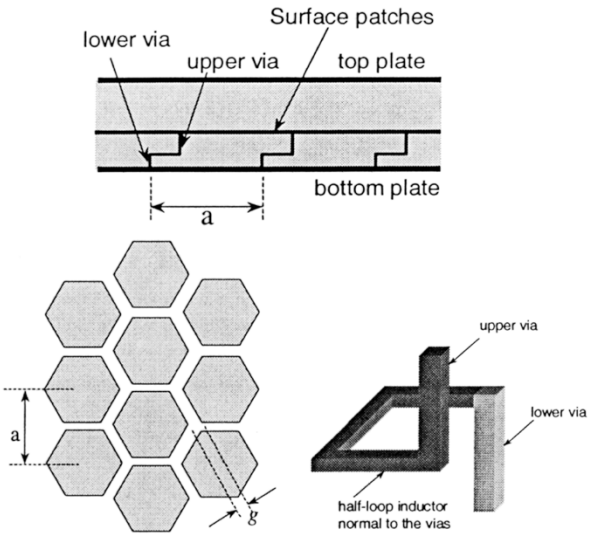

Fig. 2. Side and top views of the HIS. Also shown a three dimensional view of the vias and the half-loop conductor (drawing shows inductor).

(or the upper plane). This HIS consists of periodic hexagonal patches, which are connected to a solid metallic plate through two vertical vias. A half-loop conductor is introduced between the two vias on an intermediate layer as shown in Fig. 2. The hexagonal patch has been analyzed and modeled in [4] as parallel LC resonators. It is well known that increasing the inductance of a parallel LC resonant circuit decreases its resonant frequency while increasing its fractional bandwidth. Depending on the size of the patches, the intermediate conductor, which is in effect an inductor, can be constructed to have more (or even less) than one turn and can also be distributed on several layers without impacting the periodicity of the high-impedance surface.

This new concept of extending the conductor in the direction perpendicular to the via achieves the following two important objectives: 1) It allows increased inductance without increasing the overall PCB thickness. 2) It introduces a degree of freedom that allows fine-tuning of the inductance while keeping the capacitance constant.

III. Numerical Simulation and Discussion

To validate the new power plane concept, several full wave simulations were performed using the finite element method (FEM) code HFSS from Ansoft. The test structures consist of a 10×10 cm board with a thickness of 1.54 mm, and relative dielectric constant of 4.4. The noise source is placed at the center of the board with coordinate (5 cm, 5 cm) and the load is placed at (5 cm, 2 cm). The simulation is performed for the board without decoupling capacitance and then with eight decoupling capacitors spread around the noise source as in [5]. The transmission coefficient S12 calculated by HFSS is presented in Fig. 3 along with a comparison to experimental measurements performed in [5]. The purpose of this simulation is only intended to validate the S12 calculation procedure, and furthermore, to emphasize that good SSN mitigation can be achieved only up to about 400 MHz, due to predominant inductance from the capacitor leads.

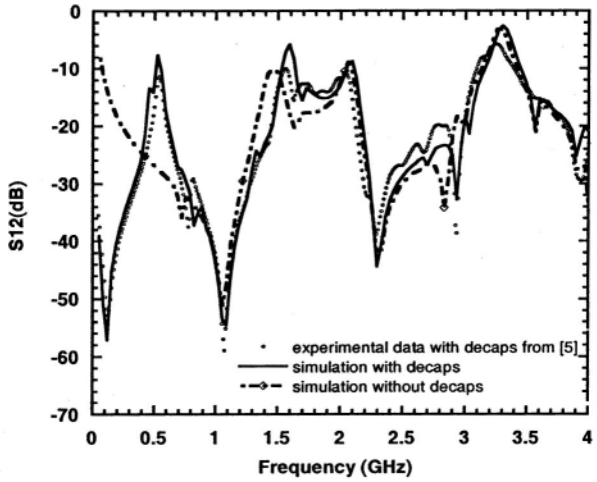

Fig. 3. Impact of decoupling capacitor on power plane resonance.

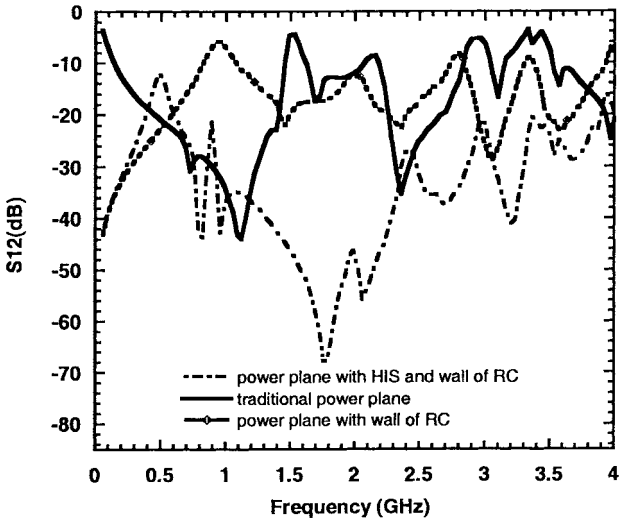

Fig. 4. Transmission characteristics S12 (in decibels) of power plane with different noise mitigation techniques.

In Fig. 4, we present the insertion loss S12 for the power plane having the HIS introduced in this work. The vias are of length 1 mm. The periodicity of the lattice, a, is 10 mm and the gap between the hexagonal patches, g, is 0.4 mm. The top plate is placed 1mm above the patches. The transmission characteristics S12 is plotted together with those of a simple parallel-plate structure of same height with and without a wall of RC pairs placed around the edges of the board (the inductance of the capacitor leads, L_c is included as before). A total of 40 RC pairs were uniformly placed around the PCB, with $R = 5.36\Omega$ and $C = 1$nF and $L_c = 0.5$nH. The resistance of the RC combination is selected to match the impedance of the simple parallel-plate system as in [1]. The wall of capacitors offers a good SSN mitigation capability at lower frequencies. For higher frequencies, however, the noise suppression capability of the HIS is remarkable. In fact, the frequency width of the resulting -20dB band-gap is approximately 3.3 GHz. Over the band-gap, the HIS significantly diminished the surface waves that travel within the plates, which in turn results in significantly reduced Q for the parallel plate cavity.

IV. Conclusion

A novel concept has been proposed to mitigate resonance in power planes. The new concept introduces a HIS, or a metallic electromagnetic band-gap structure, within the power planes. The HIS is designed to offer large bandwidth at microwave and radio frequencies. This is done by introducing additional inductance to the vias while maintaining both a reasonable thickness and periodicity. The combination of this technique with decoupling capacitors offers effective mitigation of SSN from dc to the GHz range, making this approach of significant interest for today and future high-speed digital system. The proposed power plane structure can easily be fabricated using existing PCB technology.

Acknowledgment

The authors would like to thank Dr. R. Henderson of Motorola SPS for her valuable comments on this paper.

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